A Pole-Zero Analysis Method Based on Signal-Flow Graphs for Analog IC

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Abstract

A method utilizing Mason’s rule to derive the poles and zeros of the analog integrated circuits (IC) system separately based on the signal-flow graphs (SFG) is described in this paper. The numerator and denominator of transfer function can be derived separately through simple addition and subtraction to the forward-path gains and the loop gains of the SFG by this method. Besides, the poles and zeros can be obtained by some critical loop gains and forward-path gains. The number of the nontouching loops observed intuitively from the SFG determines the order of the transfer function as well as the number of the poles and zeros. Compared to the general Kirchhoff’s voltage law (KVL) and Kirchhoff’s current law (KCL), this method reduces the amount of manual calculation considerably. Also, the circuit parameters forming poles and zeros can be obtained based on its converted SFG. In addition, it is helpful to further understand the formation of poles and zeros. The nested-miller frequency compensation (NMC), a three-stage operational amplifier, as an example, is presented to illustrate the specific application of this method.

Key Words: Mason’s Rule, Signal-Flow Graphs (SFG), Loop Search, Poles and Zeros

1. Introduction

With the development of IC fabrication technology, the supply voltage decreases. When the supply voltage drops below 1V, more stages are required as the cascading is no longer possible. Also, many operational amplifiers with three stages are required in many applications. For example, class AB amplifiers have an output stage which provides little gain but a lot of current. The first two stages are now needed to provide gain. However, the pole-zero analysis of the three-stage amplifiers [1–4] is less obvious than the two-stage amplifiers. It is more complicated to get the poles and zeros by using KCL and KVL. In order to reduce the computational complexity, Mason’s rule [5,6], based on the SFG, is utilized to derive the poles and zeros of the analog IC system. In [7], the poles and zeros are obtained after the common denominator for the transfer function. However, in this paper, the common denominator is not needed. The numerator and denominator of transfer function can be obtained separately through some critical loop gains and forward-path gains. So the parameters determining the poles and zeros can be easily obtained and the designers can analyze and adjust the circuits more efficiently. Besides, the modeling of the power electronic systems can also be simplified through SFG [8,9]. A NMC amplifier in [2] is used as an example to present the application process of this method. The poles are decided by the loops while the zeros are decided by the forward paths and the loops which are nontouching with the forward path. The dominant pole is decided by the maximum loop gain, and the nondominant pole and the third pole can be estimated through the maximum product of gains of two nontouching loops and three nontouching loops, respectively. Similarly, the DC gain and the zeros can be derived from the forward-path gains. Hence, only
some critical loops and forward paths are needed to estimate the poles and zeros.

There are six sections in this paper. Section 2 introduces the theory for analyzing the circuits on the SFG. A method for searching the loops and forward paths comprehensively is illustrated in section 3. Section 4 describes the transformation from symbolic network to SFG with an example. The pole-zero analysis of the example mentioned in section 4, utilizing the method mentioned in section 3, is shown in section 5. Section 6 is the conclusion of the method utilizing Mason’s rule to derive the poles and zeros of the analog integrated circuits system based on the SFG.

2. The Circuit Analysis Theory Based on SFG

The method utilizing SFG to analyze the circuits is based on the theory of block diagram, SFG, and Mason’s rule. The block diagram is the graphical representation of the function feature and signal direction of each module in the system. It consists of block, signal line, measurement point and summing point. Figure 1 is the basic block diagram of a feedback control system and its transfer function $T(s)$ is

$$T(s) = \frac{C(s)}{R(s)} = \frac{G(s)}{1 + G(s)H(s)}$$  \hspace{1cm} (1)

Here $C(s)$ is the input node, $R(s)$ is the output node, $G(s)$ in (1) is the forward paths function, $1 + G(s)H(s)$ is the characteristic equation of the system. $G(s)H(s)$ is the function of the open loop system.

An SFG is constructed by nodes and branches. Nodes are used to represent variables. Branches are the line segments that connect the nodes together, according to the cause-and-effect equations. The branches associate branch gains and directions. A signal can transmit through a branch only in the direction of the arrow. The SFG can be obtained by corresponding to the block diagram. The input of the block diagram is converted to source nodes and the output of the block diagram is converted to the sink nodes. The boxes are converted to branches and the function in each box is the branch gain. Thus, the block diagram is converted into the SFG. The nodes in the SFG can only express the addition of variables, so the negative feedback paths need to be expressed by the negative branch gains.

After drawing out the SFG of system, the transfer function of the system that can be derived through Mason’s rule is described as

$$P = \frac{1}{\Delta} \sum_{i=1}^{n} p_i \Delta_i$$  \hspace{1cm} (2)

where $P$ is the transfer function between the source node and the sink node; $n$ is the total number of the forward paths between the source node and the sink node; $p_i$ is the gain of the $k_{th}$ forward path between the source node and the sink node; $\Delta$ is the characteristic formula of the SFG, and

$$\Delta = 1 - \sum L_1 + \sum L_2 - \sum L_3 + \cdots + (-1)^m \sum L_n$$  \hspace{1cm} (3)

where $\Sigma L_1$ is the sum of the gains of all individual loops; $\Sigma L_2$ is the sum of products of gains of all possible combinations of two nontouching loops; $\Sigma L_3$ is the sum of products of gains of all possible combinations of three nontouching loops; $m$ is the number of the loops that are nontouching with each other. $\Delta_k$ is the $\Delta$ for that part of the SFG that is nontouching with the $k_{th}$ forward path.

3. Method to Analyze the SFG

The analysis of the SFG is for the convenience of the derivation of the poles and zeros of systems. From the Mason’s rule, the pole-zero analysis depends on the search of the forward paths and loops of the SFG. This section describes a method for the fast search of the forward paths and loops of the SFG: artificial intelligence (AI) graph search strategy. This method is conducive to manual search of the SFG. When the circuit is complex, loops become complicated. Through this method, the duplication and omission of the loops can be avoided. The

Figure 1. Basic block diagram of a feedback control system.
details of the loop search are as follows:
(a) The modality of loop is \( n_i \rightarrow \ldots \rightarrow n_i, i = 1, 2, 3 \ldots \)
Each node in the loop except \( n_i \) can appear once at most and the subscript of the nodes cannot be less than \( i \). In other words, the nodes \( n_i-1, n_i-2 \ldots n_1 \) in the loop that have been considered cannot appear in the loop \( n_i \rightarrow \ldots \rightarrow n_i, i = 1, 2, 3 \ldots \)
(b) The sufficient and necessary condition of the formation of the loop is that the node \( n_i \) has both input and output branches to the nodes \( n_{i+1}, n_{i+2} \ldots \)
(c) Only one loop is considered in each cycle.
(d) Search the loops one by one from the first node \( n_1 \).

The details of the forward path search are as follows:
(a) The modality of forward path is \( R(s) \rightarrow \ldots \rightarrow C(s) \).
(b) Any node appears once at most in each forward path. From the definition of \( \Delta \), the process of searching the nontouching relationship between forward paths and loops is the same as that of searching the nontouching relationship of the loops.

The details of searching the nontouching loops are as follows:
(a) The individual loop gains are set to be expressed by \( L_{s1}, L_{s2}, L_{s3}, L_{s4} \ldots \) When judging two nontouching loops, first judge if \( L_{s1} \) has the common node with \( L_{s2}, L_{s3}, L_{s4} \ldots \) Then judge if \( L_{s2} \) has the common node with \( L_{s3}, L_{s4} \ldots \) and the rest is by analogy.
(b) When judging three nontouching loops, the loops should be found in the group of two nontouching loops and the same method as judging two nontouching loops is used.

The theory for searching the loops and forward paths of a SFG is illustrated in this section and the application of the theory is shown in section 5.

4. The Conversion from Symbolic Diagrams to Blocks Diagrams and SFG

The actual circuit elements can be generally equivalent to the symbolic diagrams. The conversion between voltage and current in the circuits can be implemented through the change between impedance and admittance. NMC, a three-stage operational amplifier, is described as an example in this section. Every stage of the operational amplifiers can be equivalent to the corresponding transconductance and resistance. In Figure 2, C1 and C2 stand for the parasitic capacitances of operational amplifier. If C1 and C2 are relatively small, the parasitic capacitances will be neglected. This can be explained by deriving \( \Delta \) from the SFG.

The conversion from the symbolic diagram in Figure 2 to the block diagram in Figure 3 is critical for the pole-zero analysis method. Because the form of block diagrams and the symbolic diagrams are different: the block diagrams have no ground that can be found in almost all symbolic diagrams of the circuits.

The main point of the conversion from symbolic diagrams to block diagrams is to express the voltage of each node and the current of each branch. The current is expressed by subtracting the nodes at both ends of a branch and the voltage is expressed by an impedance branch. At last, the voltage of each node and the current of each branch are derived and the conversion from symbolic diagrams to block diagrams is completed.

Then, the conversion from the block diagram in Figure 3 to the SFG in Figure 4 is relatively simple. The SFG can be obtained by corresponding to the block diagram. The input of the block diagram is converted to source node and the output of the block diagram is converted to sink node. The boxes are converted to branches and the
function in each box is the branch gain. Thus, the block diagram is converted into the SFG.

5. The Analysis of SFG of the NMC Operational Amplifier

In Figure 4, R(s) is the source node and C(s) is the sink node of the SFG. The dotted lines in Figure 4 represent the input parasitic capacitances of the second and third stage of the operational amplifier. It is noted that two more loops are formed in the SFG because of the two parasitic capacitances. Also, the subsequent pole-zero analysis presents the specific influence of the parasitic capacitors on the poles and zeros. Applying the method described in section 3 in Figure 4, the loop search diagram and forward path diagram are obtained in Figure 5.

The (a), (b), (c) in Figure 5 are the loop search diagrams and (d) is the forward path diagram. When searching the loops, pay attention to the nodes whose signal can only come from the nodes that have already been searched. These nodes cannot form new loops. Noting this point, the nodes n2, n4, n5, n6, n7, n8, n9 and n10 in Figure 4 would not be used to find the new loops. This simplifies the analysis of the SFG. Ten loops are obtained through the analysis:

1. \( n_1 \rightarrow n_2 \rightarrow n_1 \)

\[ L_{e_1} = - sC_1R_1 \]  

(4)

2. \( n_1 \rightarrow n_2 \rightarrow n_3 \rightarrow n_4 \rightarrow n_5 \rightarrow n_6 \rightarrow n_7 \rightarrow n_8 \rightarrow n_9 \rightarrow n_1 \)

\[ L_{e_2} = sR_2g_{m2}R_3C_{m2}R_1C_{m2} \]  

(5)

3. \( n_1 \rightarrow n_2 \rightarrow n_3 \rightarrow n_4 \rightarrow n_5 \rightarrow n_6 \rightarrow n_7 \rightarrow n_8 \rightarrow n_1 \)

\[ L_{e_3} = - sR_2g_{m2}R_3g_{m3}R_1C_{m1} \]  

(6)

4. \( n_1 \rightarrow n_2 \rightarrow n_3 \rightarrow n_4 \rightarrow n_1 \)

\[ L_{e_4} = - sR_1C_{m1} \]  

(7)

5. \( n_3 \rightarrow n_4 \rightarrow n_3 \)

6. \( n_3 \rightarrow n_4 \rightarrow n_5 \rightarrow n_6 \rightarrow n_9 \rightarrow n_10 \rightarrow n_3 \)

\[ L_{e_5} = - sR_2C_2 \]  

(8)

7. \( n_3 \rightarrow n_4 \rightarrow n_5 \rightarrow n_6 \rightarrow n_9 \rightarrow n_10 \rightarrow n_3 \)

\[ L_{e_6} = - sR_2C_{m2} \]  

(9)

8. \( n_3 \rightarrow n_6 \rightarrow n_5 \)

\[ L_{e_7} = - sR_1R_3C_{m2} \]  

(10)

9. \( n_3 \rightarrow n_6 \rightarrow n_7 \rightarrow n_8 \rightarrow n_5 \)

\[ L_{e_8} = - sR_1C_L \]  

(11)

10. \( n_3 \rightarrow n_6 \rightarrow n_7 \rightarrow n_8 \rightarrow n_5 \)

\[ L_{e_9} = - sR_1C_{m1} \]  

(12)

Figure 4. SFG of the NMC operational amplifier.

Figure 5. The loop search diagrams and forward path diagram of the SFG of NMC. (a) The loop search diagram of node n1. (b) The loop search diagram of node n3. (c) The loop search diagram of node n5. (d) The forward path diagram.
All possible combinations of two nontouching loops in the loops above are: $L_4L_6$, $L_4L_7$, $L_4L_8$, $L_4L_{10}$, $L_5L_6$, $L_5L_9$, $L_6L_7$, $L_6L_9$, $L_7L_8$, $L_7L_{10}$, $L_8L_{10}$, and $L_9L_{10}$. All possible combinations of three nontouching loops in the above loops are: $L_4L_6L_8$, $L_4L_6L_9$, $L_4L_6L_{10}$, $L_5L_6L_8$, $L_5L_6L_9$, and $L_5L_6L_{10}$. There are no four nontouching loops in the above loops. $L_1$ and $L_5$ are the loops which are formed by the parasitic capacitances. Up to now, the denominator of the transfer function, is derived. Thus, the poles can be obtained.

\[
\Delta = 1 - (L_2 + L_3 + L_4 + L_5 + L_6 + L_9 + L_{10} + L_{11} + L_{12})
\]

(13) All possible combinations of two nontouching loops in the loops above are:

\[
L_4L_6, L_4L_7, L_4L_8, L_4L_{10}, L_5L_6, L_5L_9, L_6L_7, L_6L_9, L_7L_8, L_7L_{10}, L_8L_{10}, \text{ and } L_9L_{10}.
\]

Since the number of nontouching loops is three at most, the circuit has three poles according to the equivalent symbolic diagram. The (15) above is the accurate formula. When designing the circuits, set the parameters of the expression to an approximate value and then estimate the poles and zeros. Here, assume $gm_3 > gm_2$, $CL$ is larger than $C_m_1$ and $C_m_2$, $C_1$ and $C_2$ are relatively small compared to $C_m_1$ and $C_m_2$. The parts underlined in (15) are the largest in the coefficient of each order, and the three poles can be estimated through the calculation of the underlined parts.

The poles above are in the left-hand plane. The zeros can be derived from the forward path gains. The method searching the forward paths is described in section 3. From (d) in Figure 5, three forward paths are obtained which are as follows:

1. $R(s)\rightarrow n_1 \rightarrow n_2 \rightarrow n_3 \rightarrow n_4 \rightarrow n_5 \rightarrow C(s)$ touching with each loop.
2. $R(s)\rightarrow n_1 \rightarrow n_2 \rightarrow n_7 \rightarrow n_8 \rightarrow n_5 \rightarrow n_6 \rightarrow C(s)$ nontouching with the loops of $L_{15}$ and $L_{16}$.
3. $R(s)\rightarrow n_1 \rightarrow n_2 \rightarrow n_7 \rightarrow n_8 \rightarrow n_9 \rightarrow n_{10} \rightarrow n_5 \rightarrow n_6 \rightarrow C(s)$ touching with each loop.

The gain of $k_{th}$ forward path, $p_k$ and the $\Delta$ for that part of the SFG that is nontouching with the $k_{th}$ forward path, $\Delta_k$ are as follows:

\[
p_k = -gm_1R_1gm_2R_2gm_3R_3
\]

(19)

(19) $\Delta_1 = 1$ (20)

(20) $\Delta_2 = 1 - L_{15} - L_{16} = 1 + sR_1(C_m_2 + C_1)$ (22)

(22) $\Delta_3 = gm_1R_1gm_2R_2gm_3R_3$ (23)
Thus, the numerator of the transfer function is

\[ \text{num} = p_1 \Delta_1 + p_2 \Delta_2 + p_3 \Delta_3 \]

\[ = -g_m R_c g_m R_c g_m R_c \]

\[ + s g_m R_c R_c C_{m_1} [1 + s R_c (C_{m_2} + C_z)] \]

\[ + s g_m R_c g_m R_c g_m R_c C_{m_2} \]

\[ \approx -g_m R_c g_m R_c g_m R_c \]

\[ \cdot (1 - \frac{C_{m_2}}{g_m} - \frac{s}{g_m} \frac{C_{m_1} (C_{m_2} + C_z)}{g_m g_m}) \] (25)

Then the zeros that can be estimated through the (25) are

\[ \omega_{z_1} \approx \frac{g_m}{C_{m_2}} \] (26)

\[ \omega_{z_2} \approx \frac{g_m}{C_{m_1} (1 + \frac{C_z}{C_{m_2}})} \] (27)

\( \omega_{z_1} \) is the zero in the right-hand plane and \( \omega_{z_2} \) is the zero in the left-hand plane. From the pole-zero analysis above, the poles can be estimated by these critical loop gains: \( L_{s_3}, L_{s_1} L_{s_7}, L_{s_6} L_{s_4} L_{s_8} \). The zeros can be obtained through the forward path gains \( p_1, p_2, p_3 \), and some loop gains \( L_{s_5}, L_{s_6} \).

The example of deriving the poles and zeros presents the process of utilizing Mason’s rule to analyze the analog integrated circuits based on the SFG. The poles and zeros are derived separately. Furthermore, only some critical loops and forward paths are needed to estimate the poles and zeros which affect the stability of the circuits. Many products of loop gains can be neglected. It is intuitive for us to understand the formation mechanism of the poles and the zeros. The poles are formed from the loops while the zeros are formed from the forward paths and the loops which are nontouching with the forward paths.

From the point of SFG, some amplifiers with feed forward compensations can be easily understood, such as the amplifiers nested gm-c compensation (NGCC) in [4] and multipath miller zero cancellation compensation (MMZCC) in [10]. The NGCC in [4] amplifier has two more transconductances, \( g_{mf1} \) and \( g_{mf2} \), than NMC amplifier and if \( g_{mf1} \) and \( g_{mf2} \) are chosen to be the same as their corresponding stage transconductances, zeros will be cancelled out. Besides, the poles are the same as the NMC amplifier. This can be intuitively explained from the point of SFG. Because the two more transconductances are equivalent to two more forward paths compared to the NMC amplifier and they have little influence on the loops. Also, through using the thought that adds forward paths to cancel the zeros, the structure of MMZCC amplifier can be easily understood and thought out. Through the method presented in this paper, the poles and zeros can be separately derived. Some appropriate forward paths can be added to only change the zeros and have little effect on the poles.

6. Conclusions

In this paper, a method utilizing Mason’s rule to separately derive the poles and zeros of circuits based on the signal-flow graphs (SFG) is described. From the point of the SFG, the positions where the poles and zeros generate and the parameters related to them can be obtained more intuitively. Thus, it can help us adjust the stability of circuits efficiently. The analysis of a three-stage operational amplifier is illustrated in this paper, which presents the process of the application of the method. The method illustrated the mechanism of the formation of poles and zeros to a certain degree through this method. The poles are formed from the loops while the zeros are formed from the forward paths and the loops which are nontouching with the forward paths.

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References


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