The Oscillator Using a Single DVCC

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Abstract

The configuration of the oscillator using a single differential voltage current conveyor (DVCC) is introduced in this paper. The circuit is mainly composed of a DVCC, two resistors and two grounded-capacitors. Nevertheless, the configuration is proper for VLSI implementation due to the grounded-capacitors. The Hspice simulation results are obtained by using UMC 0.5 μm technology process parameters.

Key Words: Oscillator, DVCC, Sensitivity, Total Harmonic Distortion, Frequency Stability Factor

1. Introduction

The oscillators play an important role in analog circuit design, because they are widely used in communication, signal processing and control systems. The oscillators can be implemented in various approaches [1-3]. However, in this paper, we try to present the configuration of the oscillator using a differential voltage current conveyor (DVCC) and some other passive elements.

The second-generation current conveyor (CCII) [4] is a three-port active element, which is characterized by the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{1}$$

where '±' denote positive and negative types of CCII, respectively. The symbol of the CCII is shown in Figure 1.

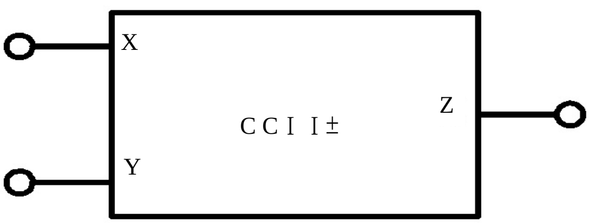

Figure 1. The CCII symbol

It is well known that the CCII introduced by Sedra and Smith has a better performance at high frequency. While a DVCC developed by Elwan and Soilman [5] is more versatile and flexible than a CCII.

In this paper, the authors use a DVCC as the building block to implement grounded-capacitors oscillator and use the signal flow graph technique to analyze the oscillator, and then verify if it is suitable for IC implementation. The simulation results for this circuit were demonstrated through Hspice with UMC 0.5 μm technology process parameters.

2. Circuit Description

The DVCC has five ports and is described by the following matrix equation:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \tag{2}$$

The CMOS realization of the DVCC+ and the symbol are shown in Figures 2 and 3 [6], respectively. The characteristics of the DVCC+ are: $I_X = I_{Z+}$; $V_X = V_{Y1} - V_{Y2}$; $I_{Y1} = I_{Y2} = 0$.

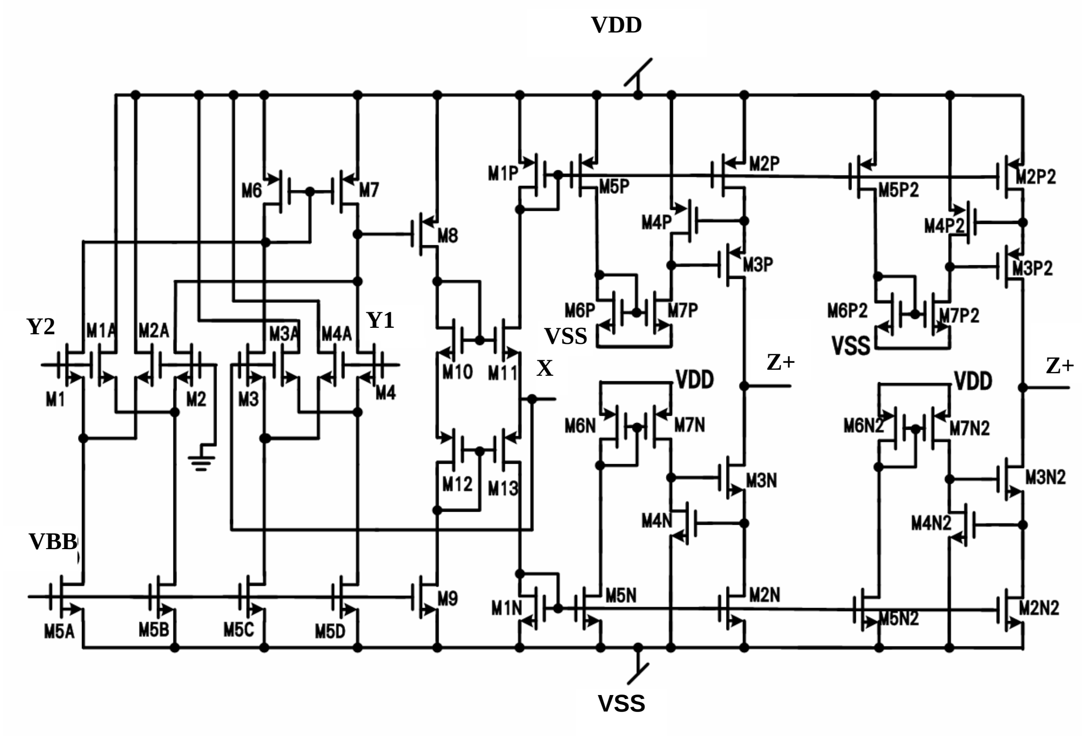

Figure 2. CMOS DVCC+ realization [6]

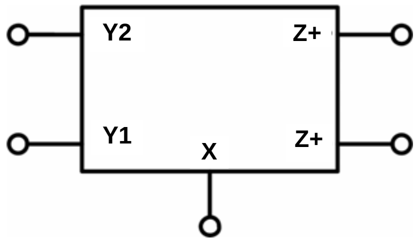

Figure 3. The DVCC+ symbol

Moreover, there is the configuration of the oscillator that has been introduced in Figure 4. Refer to the oscillator, a signal flow graph with two feedback loops is shown in Figure 5.

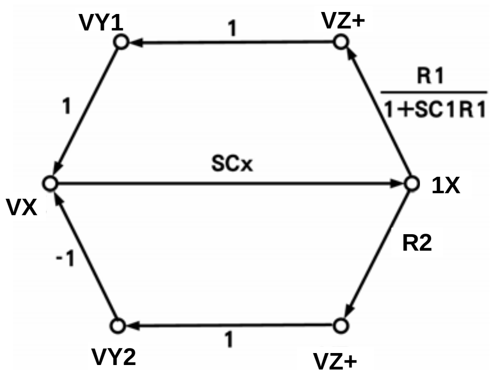

Figure 5. Two feedback loops of the oscillator

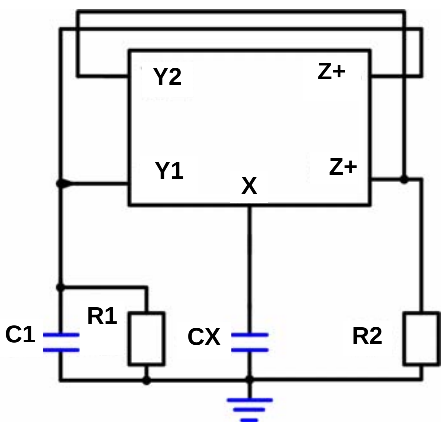

Figure 4. The configuration of the oscillator

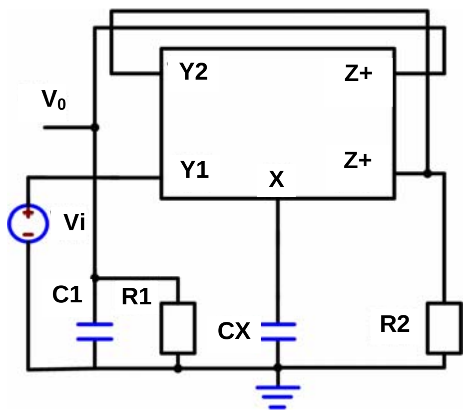

Figure 6. Determination of the loop gain of the feedback loop in Figure 4

Sinusoidal oscillator circuits are normally analyzed by determining an open loop transfer function obtained by breaking a feedback path and finding T(s) = V_o/V_i shown in Figure 6.

Refer to Figure 6, we open the feedback loop by breaking the connection of Y1 to the feedback network and apply a test signal (V_i). According to Kirchhoff loop equation and the characteristics of the DVCC+, we can obtain the signal flow graph shown in Figure 7.

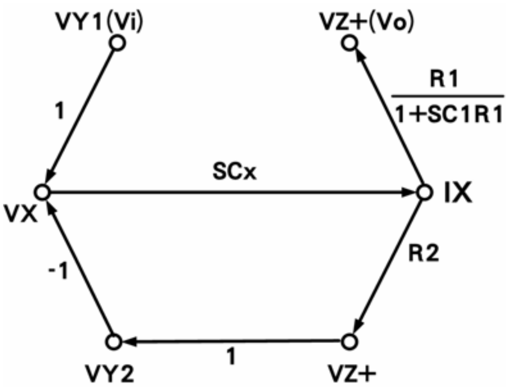

Figure 7. The signal flow graph of the open loop network

Nevertheless, the transfer function for the configuration can be easily derived from Figures 6 and 7 and formed as

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{(\frac{1}{R1} + SC1)(R2 + \frac{1}{SCx})} \tag{3}$$

It is necessary to transfer Eq. (3) to the frequency domain by putting s = jω

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1}{(\frac{R2}{R1} + \frac{C1}{Cx}) + j(\omega C1R2 - \frac{1}{\omega CxR1})} \tag{4}$$

Additionally, the Barkhausen criterion [3] can be used to obtain the condition of oscillation (CO) and frequency of oscillation (FO) from Eq. (4) which are given by:

$$\text{CO:} \quad \frac{R2}{R1} + \frac{C1}{Cx} \cong 1 \tag{5}$$

$$\text{FO:} \quad \omega_o = \frac{1}{\sqrt{C1CxR1R2}} \tag{6}$$

3. Simulation Results

The circuit of Figure 4 is simulated through Hspice with UMC 0.5um process parameters. The DC supply voltages are ± 3.3V. The passive elements are selected as R2 = 1.9 kΩ, R1 = 10 KΩ, C1 = 8 nF, and Cx = 10 nF.

Figure 8 shows the simulation results. In this simulation condition, we take the X-terminal as the output to avoid loading effect. The oscillation frequency for the configuration is about 4 kHz shown in Figure 9.

Obviously, the theoretical oscillation frequency from Eq. (6) is 4.082 kHz and its simulation values existing some deviations around 2% for Figure 4.

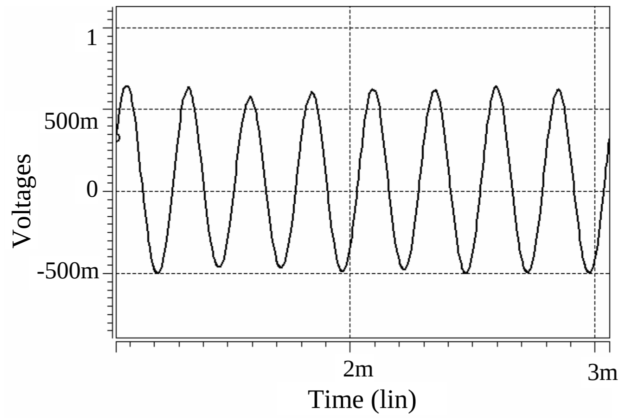

Figure 8. The simulation result of the oscillator

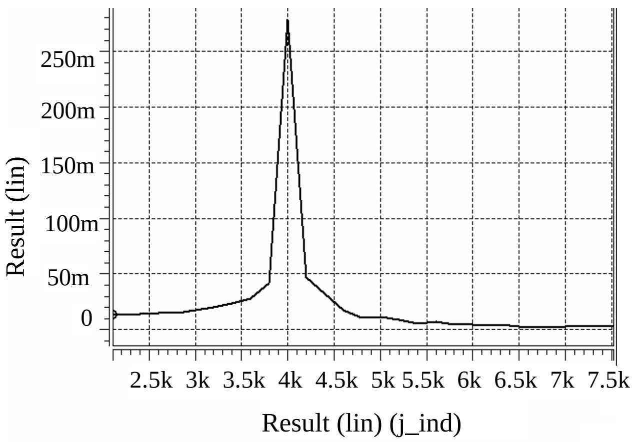

Figure 9. Oscillation frequency

4. Sensitivity Analysis, Total Harmonic Distortion and Frequency Stability

However, it is important to take the sensitivities into account when we design the oscillator. Therefore, by defining the sensitivity of the oscillation frequency ω_0 to the parameter x by

$$S_x^{\omega_0} = \frac{x}{\omega_0} \frac{d\omega_0}{dx}$$

The sensitivities of the oscillation frequency to the variations of the resistances and the capacitances can be calculated. Therefore, the different passive sensitivities of ω_0 are specified in the following equations:

$$S_{C1}^{\omega_0} = S_{Cx}^{\omega_0} = S_{R1}^{\omega_0} = S_{R2}^{\omega_0} = -\frac{1}{2} \quad (7)$$

According to above equations and the passive elements we choose, the sensitivity can be found as

$$\left|S_x^{\omega_0}\right| < 1 \ (x \in \{C1, Cx, R1, R2\}) \quad (8)$$

To proceed further, it is worth mentioning that the harmonic distortion (HD) issue should be considered when the performance is concerned. The Fourier analysis of the output wave indicates the HD of the oscillator by using Hspice. These results of the Fourier analysis are listed in Table 1, while the fundamental frequency is 4 kHz.

Table 1. Summary lists of Fourier analysis for Figure 4

Harmonic No.	Frequency (kHz)	Fourier Component (m)	Normalized Component (m)	Phase (deg)	Normalized Phase (deg)
1	4.0000	481.3728	1.0000	− 83.1427	0
2	8.0000	12.3622	25.6811	127.2927	210.4354
3	12.0000	8.4282	17.5086	− 164.9118	− 81.7691
4	16.0000	3.6773	7.6392	− 147.3961	− 64.2534
5	20.0000	2.7337	5.6790	171.7805	254.9232
6	24.0000	0.9548368	1.9836	173.1577	256.3004
7	28.0000	0.4803613	0.9978986	176.1389	259.2816
8	32.0000	0.7937113	1.6488	− 92.5356	− 9.3929
9	36.0000	1.2638	2.6255	− 110.0433	− 26.9006

Total harmonic distortion = 3.2730 percent

We can observe that the value of THD is within the reasonable range.

Using the definition of the frequency stability factor (S_F) as in [7],

$$S_F = \left.\frac{d\Phi(u)}{du}\right|_{u=1} \omega$$

where u = ω/ω o is the normalized frequency and Φ(u) S_F sents the phase function of the open loop tı (S_F) r function. The stability factor S_F can be obtained to be

$$S_F = \frac{2\sqrt{C_1 C_X R_1 R_2}}{(C_X R_2 + R_1 C_1)} \quad (9)$$

It is obviously to find the value of S_F .

5. Conclusion

In this paper, we introduce the configuration that uses DVCC+ as the building block, two grounded-capacitors and two resistors. The oscillator is useful when single-frequency oscillator is required. Because of the grounded-capacitors, the configuration is suitable for IC implementation. The performance of the oscillator has been verified by using Hspice simulation.

A new oscillator has been introduced which offers the following features: (i) use of only a single active building block;(ii) use of only two grounded-capacitors and two resistors; (iii) it has a simpler structure and is easier to analyze in comparison with [9].

References

[1] Liu, S. I. and Tsay, J. H., "Single-resistance-controlled Sinusoidal Oscillator Using Current-feedback-amplifiers," *Int. J. Electron.*, Vol. 80, pp. 661-664 (1996).

[2] Hou, C. L., "Single-element Controlled Oscillators Using Single FTFN," *Electron. Lett.*, Vol. 32, pp. 2032-2033 (1996).

[3] Barthelemy, H., Meillere, S. and Kussener, E., "CMOS Sinusoidal Oscillator Based on Current-controlled Current Conveyors," *Electron. Lett.* Vol. 38, pp. 1254-1256 (2002).

[4] Sedra, A. S. and Smith, K. C., "A Second Generation Current Conveyor and Its Applications," *IEEE Trans*., CT-17, pp. 132-134 (1970).

[5] Elwan, H. O. and Soliman, A. M., "Novel CMOS Differential Voltage Current Conveyor and Their Applications," *IEEE Proc. — Circuits Devices Syst.*, Vol. 144, pp. 195-200 (1997).

[6] Ibrahim, M. A. and Kuntman, H., "High Linearity CMOS Differential Difference Current Conveyor (DDCC)," *IEEE Proc. of the 14th International Conf. on Microelectronic*, Dec., pp. 6-9 (2002).

[7] Sedra, A. S. and Smith, K. C., *Microelectronic Circuits*, Oxford University Press, NY, U.S.A., 4th Ed., pp. 975-976 (1998).

[8] Liu, S. I., "Single-resistance-controlled Sinusoidal Oscillator Using Two FTFNs," *Electron. Lett.* Vol. 33, pp.1185-1186 (1997).

[9] Gupta, S. S. and Senani, R. "Grounded-capacitor Current-mode SRCO: Novel Application of DVCC," *Electron. Lett.* Vol. 36, pp. 195-196 (2000).

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