High-Speed Transition Detecting Circuits for On-Chip Interconnections

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Abstract

A transient sensitive trigger (TST) was used to reduce the RC delay time of the long interconnection in deep sub-micron (DSM) processes. The conventional TST circuit exhibits a voltage drop in threshold voltage during transitions, extending the delay time. This paper proposes new circuits called transition detecting circuits (TDCs) to overcome the drawbacks of the conventional TST. The proposed circuits yield 45–74% shorter delay time than the conventional TST simulation using a 0.25 μm CMOS process. The experiment results also show that the proposed TDCs are faster than the conventional TST. The proposed circuits can be applied to receiving long interconnect signals in high-speed VLSI design.

Key Word: High-Speed, Interconnections, Receivers, Deep Sub-Micron, Transition Detection

1. Introduction

The development of semiconductor manufacturing processes has reduced the sizes of devices. This trend decreases the gate delay of the integrated circuit. On one hand, more devices are being integrated in a single chip. On the other hand, a single chip contains a whole system, increasing the area of the chip. The trend results in longer wires between devices as the chips become larger. However, the interconnections are scaled down largely in the horizontal dimension as the process is scaled down, and the vertical dimension is only slightly scaled down. Hence, the interconnect delay dominates the whole chip delay in current VLSI [1–3].

Several modern technologies have been applied to reduce the interconnect delay. Aluminum used in the interconnections can be replaced with less resistive metals, such as copper. Substances with a lower dielectric constant (low-k) can be used as inter-level dielectric materials [4, 5]. Therefore, the parasitic resistance and capacitance of the wire can be reduced. Inserting repeaters (buffers) can also reduce the interconnect delay [6–8]. However, the repeaters are large devices so that it may consume more power and require a large chip area. Besides, inserting repeaters requires a CAD tool to determine their positions. Using a special receiver to receive the long interconnect signal also efficiently reduces the interconnect delay [9–12]. The other method is to insert an accelerator [10] in the middle of the interconnection to increase the driving current in the long wire.

A transient sensitive trigger (TST) reported in [10] was used to reduce the RC delay time of the long interconnection. The conventional TST circuit exhibits a voltage drop in threshold voltage during transitions resulting in longer delay time. This paper proposes three new circuits to solve the problem of the conventional TST [10] and to reduce the long interconnect delay [13]. The rest of this paper is organized as follows. Section 2 analyzes the problem of the conventional TST. The speed limitation of the TST is also considered. Section 3 pres-
ments the proposed transition detection circuits (TDCs). Section 4 compares the simulation and experiment results. The final section draws some conclusions.

2. Problem of Conventional Transient Sensitive Trigger

Figure 1 depicts the circuit diagram of the conventional transient sensitive trigger (TST) [10]. Figure 2 plots the waveforms of the TST. Initially, nodes IN and CO are assumed to be at VDD and node OUT is assumed to be at GND. The source and the gate voltages of the transistor N2 are VDD. The transistor N2 remains off at this moment. After the node IN makes a high-to-low transition between time t1 to t2, shown in Figure 2, node INP does not immediately follow. As node IN is pulled down to VDD-Vtn, the Vgs of the transistor N2 exceeds Vtn, turning on transistor N2. Finally, node INP follows IN and starts to be pulled down. The drawback of the TST is that node INP must wait till node IN has a voltage drop Vtn to turn on transistor N2. The signal INP is delayed for time (t2-t1) before turning on transistor N2.

Control signal COB is delayed by a Schmitt Trigger circuit, which also receives signal IN. At time t3, control signal CO makes a high-to-low transition, turning on transistors P2 and P3 and turning off transistors N2 and N3. Then, the internal nodes are set to the required initial state. The TST is ready to receive the next low-to-high transition of node IN. As node IN makes a low-to-high transition, the TST undergoes the required threshold voltage drop between t4 to t5 to turn on transistor P2. Hence, the speed of the conventional TST is limited.

3. Transition Detecting Circuits

The proposed transition detecting circuit (TDC), shown in Figure 3, is similar to the conventional TST circuit shown in Figure 1, except in that transistors N2 and P2 are interchanged and the control signals are inverted.

Figure 4 plots the waveforms of the TDC shown in Figure 3. Initially, the initial states of nodes IN and CO are assumed to be at VDD and that of nodes OUT and COB are assumed to be at GND. At this moment, |Vgs| of transistor P2 is VDD, which greatly exceeds |Vtp|. As node IN makes a high-to-low transition, node INP follows node IN immediately through transistor P2. Similarly, as node IN makes a low-to-high transition, node INN immediately follows node IN through transistor N2. Therefore, the TDC in Figure 3 overcomes the
drawback of the TST in Figure 1. However, the voltage swings at nodes INP and INN are from VDD to |Vtp| and from VDD- Vtn to GND, respectively. The reduced swings result in a lower |Vgs| of transistors P4 and N4 and a lower output driving current. Thus, the speed can be limited if the output load of the TDC is large.

Figure 5 depicts another transition detecting circuit of type-2. The proposed circuit in Figure 5 combines the circuit in Figure 1 and the circuit in Figure 3. Two complementary transmission gates TR1 and TR2 are used to replace transistors N2 and P2 in Figure 1 or to replace transistors P2 and N2 in Figure 3. Therefore, the transitions of nodes INN and INP in Figure 5 follow the transition of node IN. Moreover, they exhibit a full voltage swing of nodes INN and INP. In addition, the output current of the TDC in Figure 5 is not limited.

Figure 6 depicts the other transition detecting circuit of type-3. The proposed circuit in Figure 6 consists of the circuit in Figure 3 and two feedback paths. The feedback-control accelerating devices, which consist of transistors P5, P6, N5 and N6, are used to form feedback paths from node OUT to node INP and node OUT to node INN, respectively. Figure 7 plots the waveforms of the TDC shown in Figure 6. At time t1, node IN starts to make a high-to-low transition, and node INP immediately follows node IN. At time t2, the voltage at node OUT is high enough to turn on transistor N6. Therefore, another pull-down path of node INP is generated through transistors N6 and N5 to GND. At time t3, control signals...
CO and COB make transitions to turn on transistor P3 and turn off transistor N3. At time t4, node IN starts to make a low-to-high transition, and node INN immediately follows node IN. At time t5, the voltage at node OUT is low enough to turn on transistor P6. Therefore, another pull-up path of node INN is generated through transistors P6 and P5 to VDD. At time t6, control signals CO and COB make transitions to turn on transistor N3 and turn off transistor P3. Using the accelerating circuit, full voltage swings are generated at nodes INN and INP. Furthermore, transitions at nodes INP and INN are accelerated through the feedback paths. Figure 7 indicates that node INP makes a sharp transition at t2 and node INN makes a sharp transition at t5, because of the feedback accelerating paths, increasing the speed of transmission of node IN to nodes INP and INN.

4. Experiment Results

A 1P5M 0.25 μm CMOS device model is used for SPICE simulation. Figure 8 depicts the benchmark circuit that consists of a driver, a three-segment RC wire model and a receiver. The driver is a simple static inverter. The parasitic resistance and capacitance of the metal-1 wire in the 0.25 μm CMOS process are 238 Ω/mm and 0.239 pF/mm, respectively.

Figure 9 shows the simulated delays for interconnections of different lengths. The delay is measured from node IN to node OUT, as shown in Figure 8. The inverter is sized to its optimum delay performance. As shown in Figure 7, Waveforms of the TDC in Figure 6.

Figure 6. Transition detecting circuit, type-3.
Figure 9, the delay of the proposed circuits (Figures 3, 5 and 6) is shorter than that of the conventional TST. Table 1 compares the gate delays of the conventional TST and the proposed TDCs. The gate delays are measured from the receiver input to the receiver output. Compared to the conventional TST, the TDCs in Figures 3, 5, and 6 reduce the gate delay by 47%, 45% and 74%, respectively.

Figure 10 shows the power consumption for different lengths of interconnection. The power consumption includes that of the interconnection, the driver and the receiver. The frequency of the input signal is chosen to be 12.5 MHz to guarantee a full-voltage swing at the input node IN of the receiver. The power consumption of the conventional TST and the TDCs exceeds that of the static inverter because the control signal of the conventional TST and the TDCs is generated by a Schmitt Trigger cir-

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**Table 1.** Gate delay for different receivers

<table>
<thead>
<tr>
<th></th>
<th>Gate delay (ps)</th>
<th>Normalized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 1</td>
<td>380</td>
<td>1.00</td>
</tr>
<tr>
<td>Figure 3</td>
<td>200</td>
<td>0.53</td>
</tr>
<tr>
<td>Figure 5</td>
<td>210</td>
<td>0.55</td>
</tr>
<tr>
<td>Figure 6</td>
<td>130</td>
<td>0.26</td>
</tr>
<tr>
<td>Inverter</td>
<td>780</td>
<td>2.05</td>
</tr>
</tbody>
</table>

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**Table 2.** Comparisons of the conventional TST and the TDCs

<table>
<thead>
<tr>
<th></th>
<th>Speed</th>
<th>Power</th>
<th>Area</th>
<th>Internal Swing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 1</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Full-swing</td>
</tr>
<tr>
<td>Figure 3</td>
<td>Better</td>
<td>Good</td>
<td>Good</td>
<td>Not full-swing</td>
</tr>
<tr>
<td>Figure 5</td>
<td>Better</td>
<td>Good</td>
<td>Good</td>
<td>Full-swing</td>
</tr>
<tr>
<td>Figure 6</td>
<td>Excellent</td>
<td>Good</td>
<td>Good</td>
<td>Full-swing</td>
</tr>
<tr>
<td>Inverter</td>
<td>Poor</td>
<td>Excellent</td>
<td>Good</td>
<td>–</td>
</tr>
</tbody>
</table>

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**Figure 8.** Three segment RC distributed elements of wire for simulation.

**Figure 9.** Delays for interconnections of various lengths.

**Figure 10.** Power consumption for interconnections of various lengths.

**Figure 11.** Delays obtained with different TSAs.
Figure 12. Photograph of the test chip.

Figure 13. Measured waveforms and delays.
circuit that has large short-circuit current.

In [10], the conventional TST is applied to generate a transient sensitive accelerator (TSA) that accelerates the long interconnect signal. Figure 11 compares the delays obtained with different TSAs using the TST and the TDCs. The TSAs that use the TDCs are faster than the conventional TSA.

Table 2 compares the characteristics of the TST and the TDCs. The TDC in Figure 6 performs best in terms of speed and power dissipation. Compared to the static inverter, the TDCs may require more devices, increasing the chip area and the power dissipation. However, the increased area and power represent only a very small overhead for a large chip.

Figure 12 shows the photograph of the test chip. The test chip was implemented in a 0.25 µm 1P5M CMOS process. The area of the test chip including the I/O pads is 730 × 850 µm². In this test chip, the conventional TST (Figure 1) and the proposed circuits (Figures 3, 5 and 6) are used to receive the 10 mm metal-1 wire signals. The measured delays, including the wire, input and output buffers delays are shown in Figure 13. The measured delays are 9.15 ns, 8.05 ns, 7.95 ns and 7.45 ns for the circuits shown in Figures 1, 3, 5 and 6, respectively. The simulation delays of input and output buffers are 3.82 ns totally. The net delay of the circuits in Figures 1, 3, 5 and 6, not including the buffers delay are 5.33 ns, 4.23 ns, 4.13 ns and 3.62 ns, respectively. The results are very close to the simulation of 10 mm wires shown in Figure 9. It is verified that the proposed schemes are faster than the conventional TST.

5. Conclusions

Three transition detecting circuits (TDCs) are proposed in this paper. The proposed TDCs overcome the drawback of the conventional TST. The proposed circuits are proven to perform faster than the conventional TST. The proposed TDCs have a 45–74% delay reduction than the conventional TST simulated using a 0.25 µm CMOS process. A test chip is implemented. The experiment results also show that the proposed circuits are faster than the conventional TST. The overheads of area and power dissipation are very small for a large chip. The proposed TDCs can be applied to receive long interconnect signals in a high-speed VLSI design. Besides, the proposed TDCs are well suited to constructing an accelerator to of the interconnect signal than that of the conventional TST.

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References


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